Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A semiconductor integrated circuit for use in an audio-video device arranged to produce audio-video signals from received encrypted broadcast signals without requiring receipt of one or more transmitted keys, comprising:

an input interface for receipt of a received encrypted enable signal;

an output interface for output of audio-video signals;

one or more hardware circuit portions each arranged to process data in relation to the audio-video signals;

a first decryption circuit arranged to receive the encrypted enable signal and to decrypt the encrypted enable signal in accordance with a pre-stored key on the integrated circuit to provide a plain text message;

a store containing a stored value for the circuit;

an enabling circuit arranged to generate an enable or disable signal to selectively restrict, deny, or allow operation of at least one of the one or more hardware circuit portions; ~~and~~

a comparison circuit arranged to compare the plain text message with the stored value and to selectively instruct the enabling ~~device~~ circuit if the plain text message and stored value match; and

a second decryption circuit in the one or more hardware circuit portions and arranged to receive a common key from a common key store in the integrated circuit and to decrypt the received encrypted broadcast signal in response to receipt of the common key and the generation of the enable signal.

2. (Previously Presented) The semiconductor integrated circuit according to claim 1 wherein the enabling circuit comprises one or more switch elements arranged to

selectively interrupt a data pathway to, from, or within at least one of the one or more of the hardware circuit portions.

3. (Previously Presented) The semiconductor integrated circuit according to claim 2 wherein the data pathway is a critical data pathway, whereby interruption of the pathway prevents operation of the at least one of the one or more hardware circuit portions.

4. (Previously Presented) The semiconductor integrated circuit according to claim 2 wherein the data pathway relates to a clock of one or more hardware circuit portions, whereby interruption of the data pathway causes the clock to run slower than normal.

5. (Previously Presented) The semiconductor integrated circuit according to claim 4 wherein the one of the one or more hardware circuit portions is a main CPU of the semiconductor integrated circuit.

6. (Previously Presented) The semiconductor integrated circuit according to claim 2 wherein the at least one of the one or more hardware circuit portions is a display engine, whereby interruption of the data pathway causes the video signals at the output interface to be interrupted or impaired.

7. (Previously Presented) The semiconductor integrated circuit according to claim 2 wherein the at least one of the one or more hardware circuit portions is a data port of the semiconductor integrated circuit, whereby interruption of the data pathway prevents operation of the data port.

8. (Previously Presented) The semiconductor integrated circuit according to claim 1 wherein the input interface is arranged to receive the encrypted enable signal from a broadcast signal.

9. (Previously Presented) The semiconductor integrated circuit according to claim 1 wherein the input interface is arranged to receive the encrypted enable signal from a manual input device.

10. (Previously Presented) The semiconductor integrated circuit according to claim 1 wherein the input interface is arranged to receive the encrypted enable signal from another device.

11. (Previously Presented) The semiconductor integrated circuit according to claim 1 wherein the enabling circuit comprises a store arranged to store indications of hardware circuit elements to be restricted, denied, or allowed to operate.

12. (Previously Presented) The semiconductor integrated circuit according to claim 11 wherein the store comprises one or more hardware fuses.

13. (Previously Presented) The semiconductor integrated circuit according to claim 11 wherein the store comprises a non-volatile memory.

14. (Previously Presented) The semiconductor integrated circuit according to claim 1 wherein the enabling circuit is arranged to extract from the plain text message indications of which hardware circuit elements should be restricted, denied, or allowed to operate.

15. (Previously Presented) The semiconductor integrated circuit according to claim 1 wherein the semiconductor integrated circuit is a monolithic circuit for decryption of broadcast audio-video signals.

16. (Previously Presented) The semiconductor integrated circuit according to claim 2 wherein the at least one of the one or more hardware circuit portions relates to storing

audio-video signals to an external storage device, whereby the enabling circuit is arranged to selectively restrict, deny, or allow storage of the audio-video signals produced by the circuit.

17. (Previously Presented) The semiconductor integrated circuit according to claim 2 comprising an input for receiving broadcast signals from a broadcast network from which the audio-video signals are produced, and wherein the at least one of the one or more hardware circuit portions relates to production of the audio-video signals, whereby the enabling circuit is arranged to selectively restrict, deny, or allow production of the audio-video signals.

18. (Currently Amended) A television decoder for encrypted broadcast signals, comprising a semiconductor integrated circuit that comprises

an input interface for receipt of a received encrypted enable signal;

an output interface for output of audio-video signals;

one or more hardware circuit portions each arranged to process data in relation to the audio-video signals;

a first decryption circuit arranged to receive the encrypted enable signal and to decrypt the encrypted enable signal in accordance with a pre-stored key on the integrated circuit to provide a plain text message;

a store containing a stored value for the circuit;

an enabling circuit arranged to generate an enable or disable signal to selectively restrict, deny, or allow operation of at least one of the one or more hardware circuit portions; ~~and~~

a comparison circuit arranged to compare the plain text message with the stored value and to selectively instruct the enabling device if the plain text message and stored value match; and

a second decryption circuit in the one or more hardware circuit portions and arranged to receive a common key from a common key store in the integrated circuit and to decrypt the received encrypted broadcast signal in response to receipt of the common key and the generation of the enable signal.

19. (Previously Presented) A method of providing an audio video device to a user, the audio video device of the type for manipulation and presentation of audio video content and comprising a plurality of hardware circuit portions on a monolithic semiconductor circuit, and an input interface, the method comprising:

supplying the audio video device for an end user in a condition that one or more of the hardware circuit portions are inoperable or have reduced functionality;

arranging a subscription agreement with the end user in which the user pays for ongoing functionality of the one or more hardware circuit portions; and

providing an enable message in encrypted form for input to the input interface, the enable message instructing the monolithic semiconductor circuit to enable functionality of one of the one or more hardware circuit portions.

20. (Previously Presented) The method according to claim 19 wherein the audio-video device is a television decoder.

21. (Previously Presented) The method according to claim 20 wherein the enable message is broadcast to the audio-video device.

22. (Previously Presented) The method according to claim 20 wherein one of the plurality of hardware circuit portions is a cryptographic processor for decryption of television signals, the enable message instructing the enablement of the cryptographic processor.

23. (Previously Presented) The method according to claim 20 wherein one of the plurality of hardware circuit portions is a data port, the enable message instructing the connection or disconnection of the data port.

24. (Currently Amended) A circuit for receiving encrypted broadcast signals and producing audio-video signals therefrom, comprising:

a first decryption circuit adapted to decrypt an encrypted enable signal in accordance with a pre-stored key to output a plain text message; ~~and~~

a comparison circuit adapted to compare the plain text message with a ~~stored~~ pre-stored value and selectively output a control signal if the plain text message matches the ~~stored~~ pre-stored value; and

a second decryption circuit adapted to decrypt the encrypted broadcast signals and produce the audio-video signals in response to receipt of a pre-stored common key and the control signal.

25. (Previously Presented) The circuit of claim 24, comprising an enabling circuit adapted to selectively enable, disable, and restrict operation of at least one other circuit in response to the control signal.

26. (Previously Presented) The circuit of claim 25, wherein the enable circuit is adapted to select which of a plurality of other circuits to selectively enable, disable, and restrict operation in response to the control signal.

27. (Currently Amended) A method of controlling a circuit for receiving encrypted broadcast signals and producing audio-video signals therefrom, comprising:

decrypting an encrypted enable signal in accordance with a pre-stored key to output a plain text message; ~~and~~

comparing the plain text message with a pre-stored value and selectively outputting a control signal if the plain text message matches the pre-stored value; and

decrypting the encrypted broadcast signals and producing the audio-video signals in response to receipt of a pre-stored common key and the control signal.

28. (Previously Presented) The method of claim 27, comprising the further step of selectively enabling, disabling, and restricting operation of at least one other circuit in response to the control signal.

29. (Currently Amended) The method of claim 28, wherein ~~selectively~~ selectively enabling, disabling, and restricting operation comprises selecting which of a plurality of other circuits to selectively enable, disable, and restrict operation in response to the control signal.